

FEATURES

- 2048 by 2048 pixel format
- 13.5 μm square pixels
- Image area 27.6 x 27.6 mm
- Back Illuminated format for high quantum efficiency
- Full-frame operation
- Symmetrical anti-static gate protection
- Very low noise output amplifiers
- Dual responsivity output amplifiers
- Wide dynamic range for 15-bit operation
- Gated dump drain on output register
- 100% active area
- New compact footprint package

APPLICATIONS

- Scientific Imaging
- Microscopy
- Medical Imaging

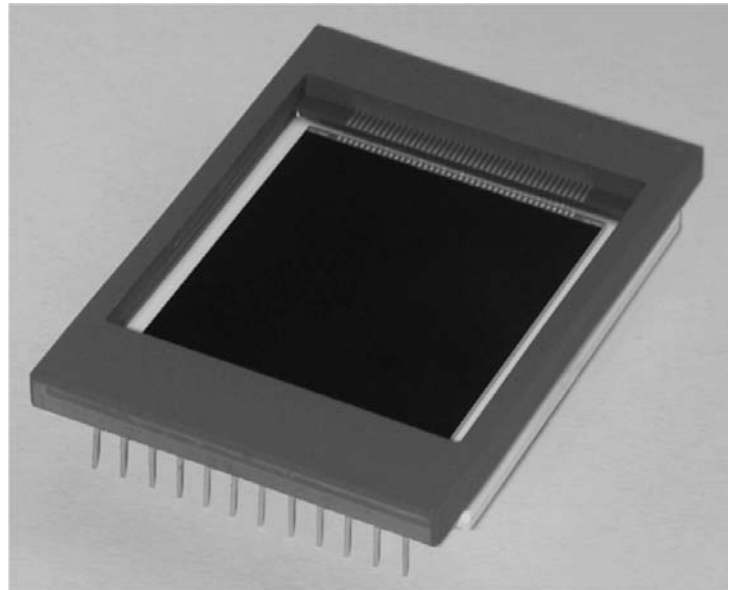
INTRODUCTION

This version of the CCD42 family of CCD sensors has full-frame architecture. Back illumination technology, in combination with extremely low noise amplifiers, makes the device well suited to the most demanding applications requiring a high dynamic range. To improve the sensitivity further, the CCD is manufactured without anti-blooming structures.

There are two low noise amplifiers in the read out register, one at each end. Charge can be made to transfer through either or both amplifiers by making the appropriate $R\phi$ connections. The readout register has a gate controlled dump drain to allow fast dumping of unwanted data.

The register is designed to accommodate four image pixels of charge and a summing well is provided capable of holding six image pixels of charge. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

Other variants of the CCD42-40 available are front illuminated format and inverted mode. In common with all e2v technologies CCD Sensors, the front illuminated CCD42-40 can be supplied with a fibre-optic window or taper, or with a phosphor coating. Designers are advised to consult e2v technologies should they be considering using CCD sensors in abnormal environments or if they require customised packaging.



TYPICAL PERFORMANCE

(Low noise mode)

| | | |
|-------------------------------|---------------------|----------------------------|
| Maximum readout frequency | 3 | MHz |
| Output amplifier responsivity | 4.5 | $\mu\text{V}/\text{e}^-$ |
| Peak signal | 150 | ke^-/pixel |
| Dynamic range (at 20 kHz) | $\approx 50\,000:1$ | |
| Spectral range | 200 - 1060 | nm |
| Readout noise (at 20 kHz) | 3 | $\text{e}^- \text{ rms}$ |

GENERAL DATA

Format

| | | |
|-------------------------------------|-------------|---------------|
| Image area | 27.6 x 27.6 | mm |
| Active pixels (H) | 2048 | |
| (V) | 2048 + 4 | |
| Pixel size | 13.5 x 13.5 | μm |
| Number of output amplifiers | 2 | |
| number of underscan (serial) pixels | 50 | |
| Fill factor | 100 | % |

Package

| | | |
|---------------------------------|-------------------|----|
| Package size | 37.0 x 51.7 | mm |
| Number of pins | 24 | |
| Inter-pin spacing | 2.54 | mm |
| Inter-row spacing across sensor | 45.72 | mm |
| Window material | removable glass | |
| Package type | ceramic DIL array | |

PERFORMANCE

| | Min | Typical | Max | |
|--|--------|-----------|--------|---------------------------|
| Peak charge storage (see note 1) | 100k | 150k | - | e ⁻ /pixel |
| Peak output voltage (unbinned) | - | 675 | - | mV |
| Dark signal at 293 K (see notes 2 and 3) | - | 20 000 | 45 000 | e ⁻ /pixel/s |
| Dynamic range (see note 4) | - | 50 000:1 | - | |
| Charge transfer efficiency (see note 5): | | | | |
| parallel | 99.999 | 99.9999 | - | % |
| serial | 99.999 | 99.9993 | - | % |
| Output amplifier responsivity: | | | | |
| low noise mode (see note 3) | 3.0 | 4.5 | 6.0 | μV/e ⁻ |
| high signal mode | - | 1.5 | - | μV/e ⁻ |
| Readout noise at 243 K: | | | | |
| low noise mode (see notes 3 and 6) | - | 3.0 | 4.0 | rms e ⁻ /pixel |
| high signal mode | - | 6.0 | - | rms e ⁻ /pixel |
| Maximum readout frequency (see note 7) | - | 20 | 3000 | kHz |
| Dark signal non-uniformity at 293 K (std. deviation) (see notes 3 and 8) | - | 2000 | 4500 | e ⁻ /pixel/s |
| Output node capacity (see note 9) | - | 1,000,000 | - | e ⁻ |

Spectral Response at 243 K

| Wavelength (nm) | Minimum Response (QE) | | | | | Maximum Response Non-uniformity (1σ) | |
|-----------------|----------------------------|-----------------------------------|-------------------------------|--------------------------------|------------------------|--------------------------------------|---|
| | Enhanced Process UV Coated | Enhanced Process Broadband Coated | Basic Process Mid-band Coated | Basic Process Broadband Coated | Basic Process Uncoated | | |
| 300 | 45 | - | - | - | - | - | % |
| 350 | 45 | 50 | 15 | 25 | 10 | 5 | % |
| 400 | 55 | 80 | 40 | 55 | 25 | 3 | % |
| 500 | 60 | 80 | 85 | 75 | 55 | 3 | % |
| 650 | 60 | 75 | 85 | 75 | 50 | 3 | % |
| 900 | 30 | 30 | 30 | 30 | 30 | 5 | % |

The uncoated process is suitable for soft X-ray and EUV applications.

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (measured at mid-clock level)

| | Min | Typical | Max | |
|--|-----|---------|-----|----|
| IØ/IØ interphase | - | 16 | - | nF |
| IØ/SS | - | 32 | - | nF |
| RØ/RØ interphase | - | 80 | - | pF |
| RØ/(SS + DG + OD) | - | 150 | - | pF |
| Output impedance at typical operating conditions | - | 350 | - | Ω |

NOTES

- Signal level at which resolution begins to degrade.
- Measured between 243 and 293 K typically. The typical average (background) dark signal at any temperature T (kelvin) between 230 K and 300 K may be estimated from:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$
 where Q_{d0} is the dark signal at 293 K.
- Test carried out at e2v technologies on all sensors.
- Dynamic range is the ratio of full-well capacity to readout noise measured at 243 K and 20 kHz readout frequency.
- CCD characterisation measurements made using charge generated by X-ray photons of known energy.
- Measured using a dual-slope integrator technique (i.e. correlated double sampling) with a 20 μs integration period.
- Readout above 3 MHz can be achieved but performance to the parameters given cannot be guaranteed.
- Measured between 243 and 293 K, excluding white defects.
- With output circuit configured in low responsivity/high capacity mode (OG2 high).

BLEMISH SPECIFICATION

Traps Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than $200 e^-$ at 243 K.

Slipped columns Are counted if they have an amplitude greater than $200 e^-$.

Black spots Are counted when they have a signal level of less than 80% of the local mean at a signal level of approximately half full-well.

White spots Are counted when they have a generation rate 25 times the specified maximum dark signal generation rate (measured between 243 and 293 K). The typical temperature dependence of white spot blemishes is the same as that of the average dark signal i.e.:

$$Q_d/Q_{d0} = 122T^3e^{-6400/T}$$

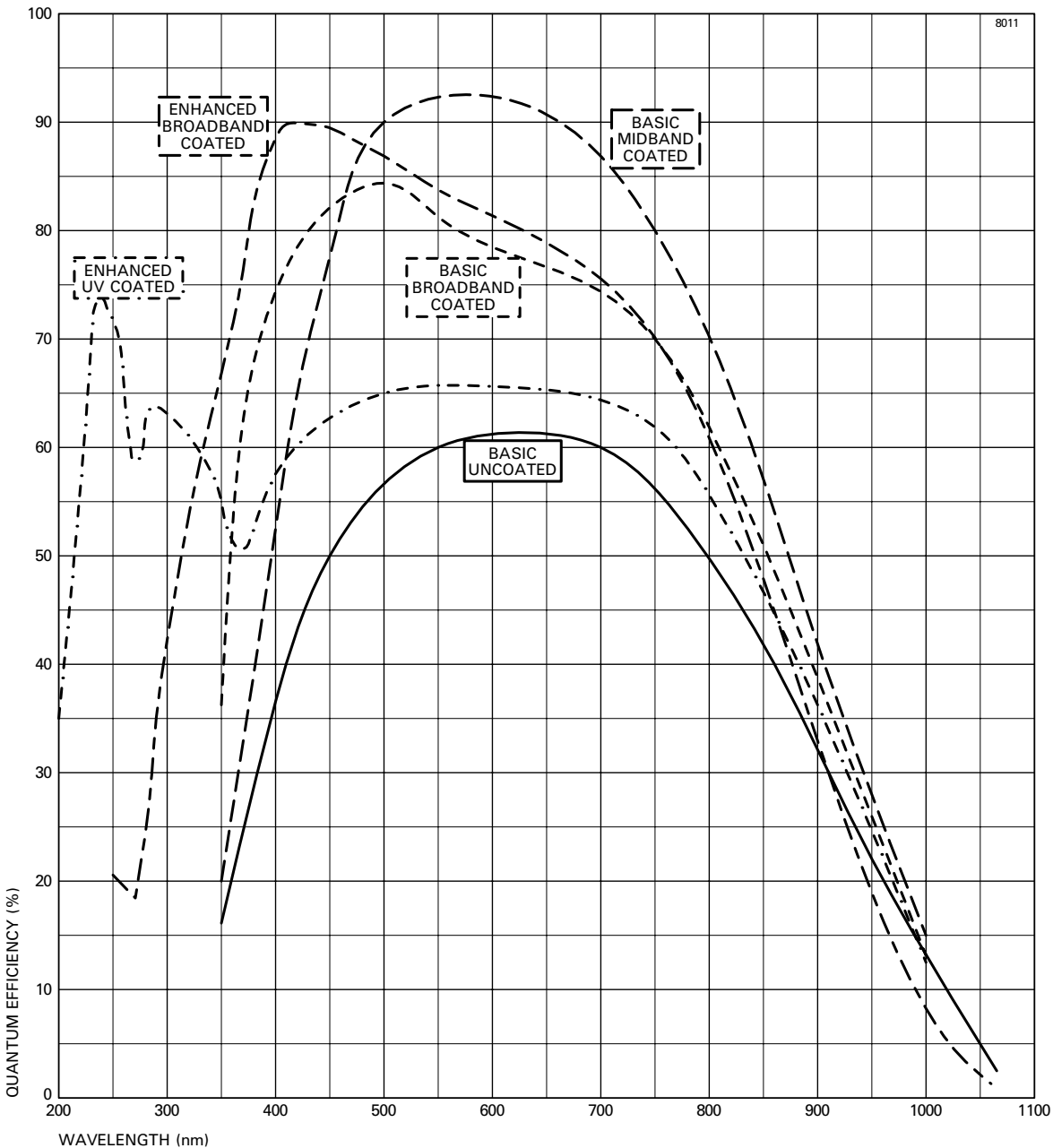
Column defects A column which contains at least 50 white or 50 black defects.

| GRADE | 0 | 1 | 2 |
|--------------------------------|-----|-----|-----|
| Column defects; black or white | 0 | 3 | 6 |
| Black spots | 100 | 150 | 250 |
| Traps $> 200 e^-$ | 10 | 20 | 30 |
| White spots | 100 | 150 | 200 |

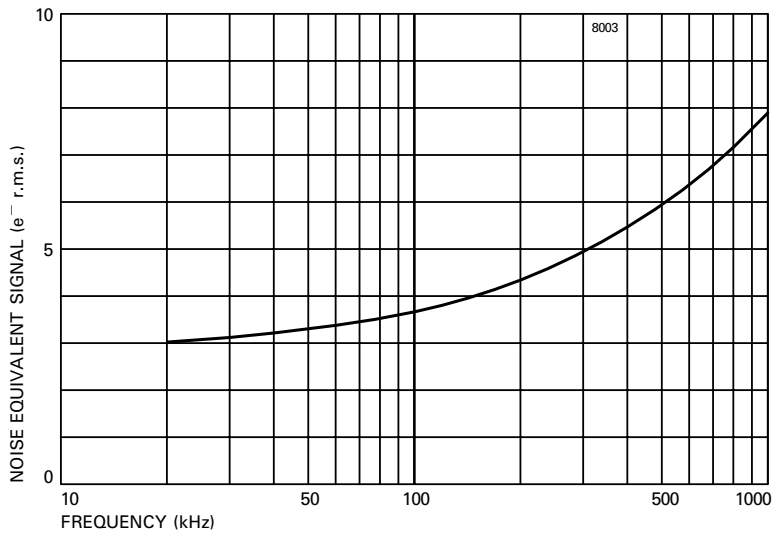
Grade 5 Devices which are fully functional, with image quality below that of grade 2, and which may not meet all other performance parameters.

Note The effect of temperature on defects is that traps will be observed less at higher temperatures but more may appear below 243 K. The amplitude of white spots and columns will decrease rapidly with temperature.

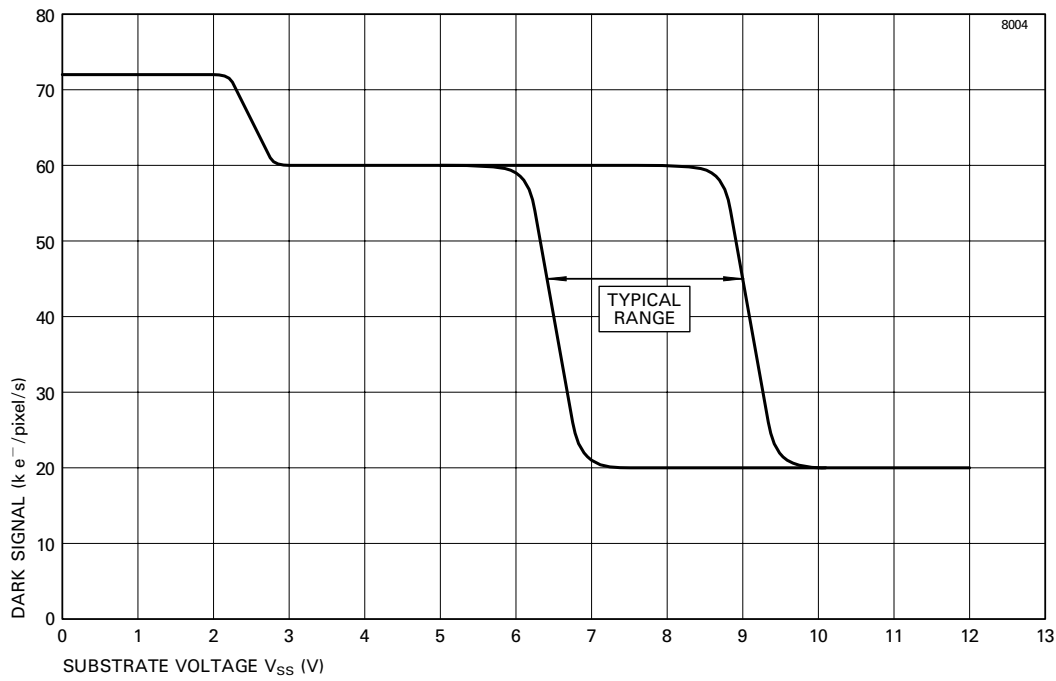
TYPICAL SPECTRAL RESPONSE (At -30°C , no window)



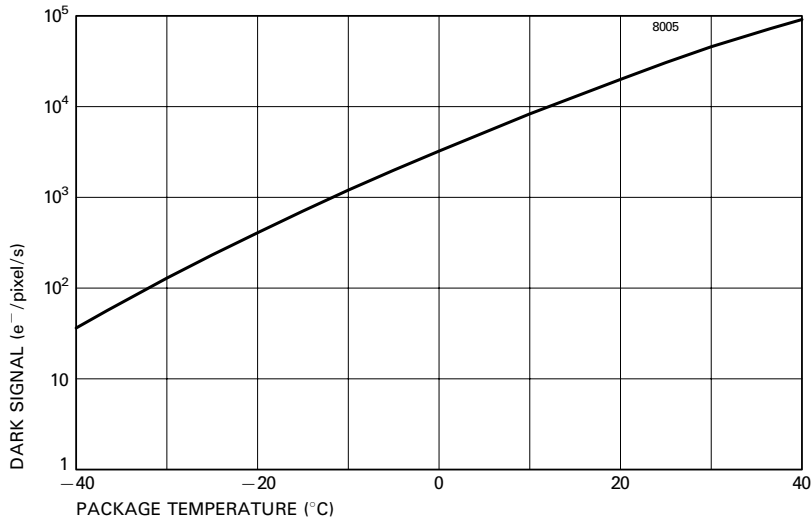
TYPICAL OUTPUT CIRCUIT NOISE (Measured using clamp and sample)



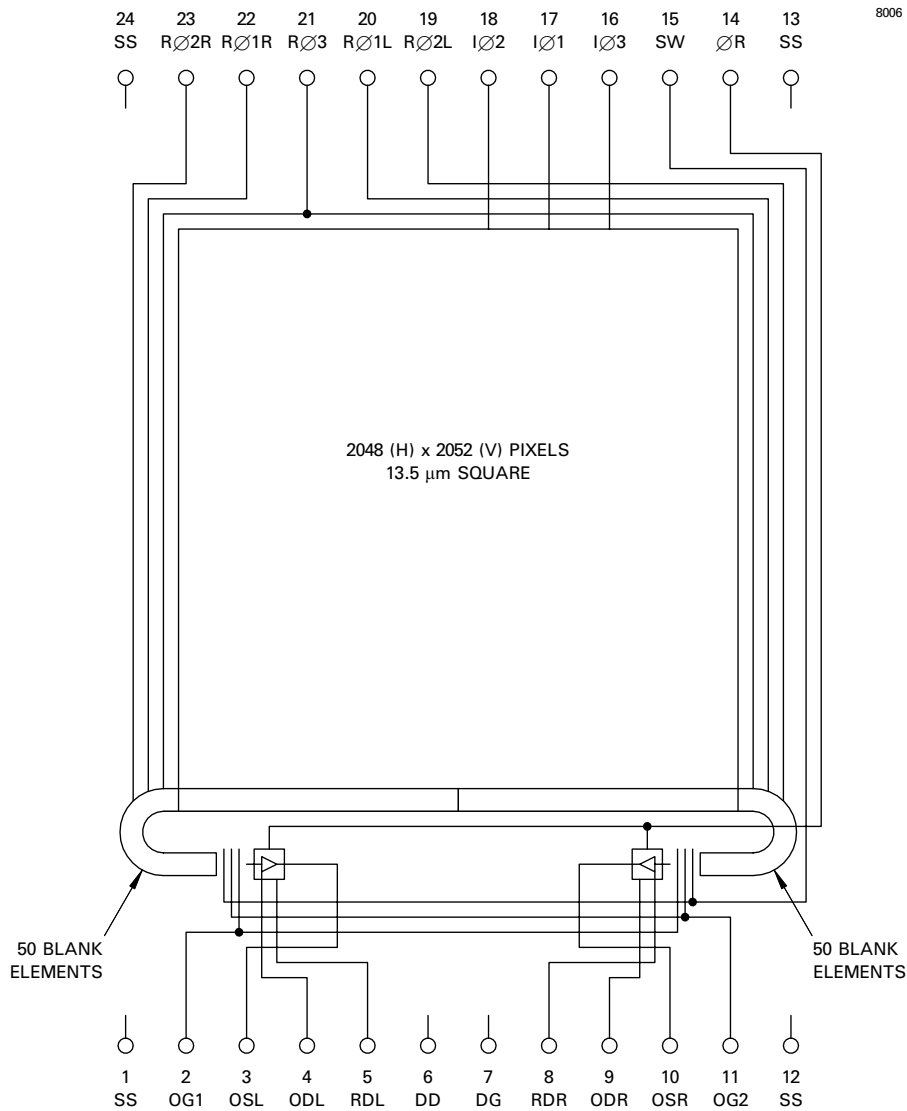
TYPICAL VARIATION OF DARK CURRENT WITH SUBSTRATE VOLTAGE



TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

| PIN | REF | DESCRIPTION | CLOCK LOW Typical | CLOCK HIGH OR DC LEVEL (V) | | | MAXIMUM RATINGS with respect to V _{SS} |
|-----|------|----------------------------------|----------------------|----------------------------|---------|-----|--|
| | | | | Min | Typical | Max | |
| 1 | SS | Substrate | n/a | 0 | 9 | 10 | - |
| 2 | OG1 | Output gate 1 | n/a | 2 | 3 | 4 | ± 20 V |
| 3 | OSL | Output transistor source (left) | n/a | see note 9 | | | -0.3 to +25 V |
| 4 | ODL | Output drain (left) | n/a | 27 | 29 | 31 | -0.3 to +25 V |
| 5 | RDL | Reset drain (left) | n/a | 15 | 17 | 19 | -0.3 to +25 V |
| 6 | DD | Dump drain | n/a | 22 | 24 | 26 | -0.3 to +25 V |
| 7 | DG | Dump gate (see note 10) | 0 | - | 12 | 15 | ± 20 V |
| 8 | RDR | Reset drain (right) | n/a | 15 | 17 | 19 | -0.3 to +25 V |
| 9 | ODR | Output drain (right) | n/a | 27 | 29 | 31 | -0.3 to +25 V |
| 10 | OSR | Output transistor source (right) | n/a | see note 9 | | | -0.3 to +25 V |
| 11 | OG2 | Output gate 2 (see note 11) | 4 | 16 | 20 | 24 | ± 20 V |
| 12 | SS | Substrate | n/a | 0 | 9 | 10 | - |
| 13 | SS | Substrate | n/a | 0 | 9 | 10 | - |
| 14 | ∅R | Reset gate | 0 | 8 | 12 | 15 | ± 20 V |
| 15 | SW | Summing well | | Clock as R∅3 | | | ± 20 V |
| 16 | I∅3 | Image area clock, phase 3 | 0 | 8 | 10 | 15 | ± 20 V |
| 17 | I∅1 | Image area clock, phase 1 | 0 | 8 | 10 | 15 | ± 20 V |
| 18 | I∅2 | Image area clock, phase 2 | 0 | 8 | 10 | 15 | ± 20 V |
| 19 | R∅2L | Register clock phase 2 (left) | 1 | 8 | 11 | 15 | ± 20 V |
| 20 | R∅1L | Register clock phase 1 (left) | 1 | 8 | 11 | 15 | ± 20 V |
| 21 | R∅3 | Register clock phase 3 | 1 | 8 | 11 | 15 | ± 20 V |
| 22 | R∅1R | Register clock phase 1 (right) | 1 | 8 | 11 | 15 | ± 20 V |
| 23 | R∅2R | Register clock phase 2 (right) | 1 | 8 | 11 | 15 | ± 20 V |
| 24 | SS | Substrate | n/a | 0 | 9 | 10 | - |

If all voltages are set to the typical values, operation at or close to specification should be obtained. Some adjustment within the range specified may be required to optimise performance. Refer to the specific device test data if possible.

Maximum voltages between pairs of pins:

pin 3 (OSL) to pin 4 (ODL) ± 15 V

pin 9 (ODR) to pin 10 (OSR) ± 15 V

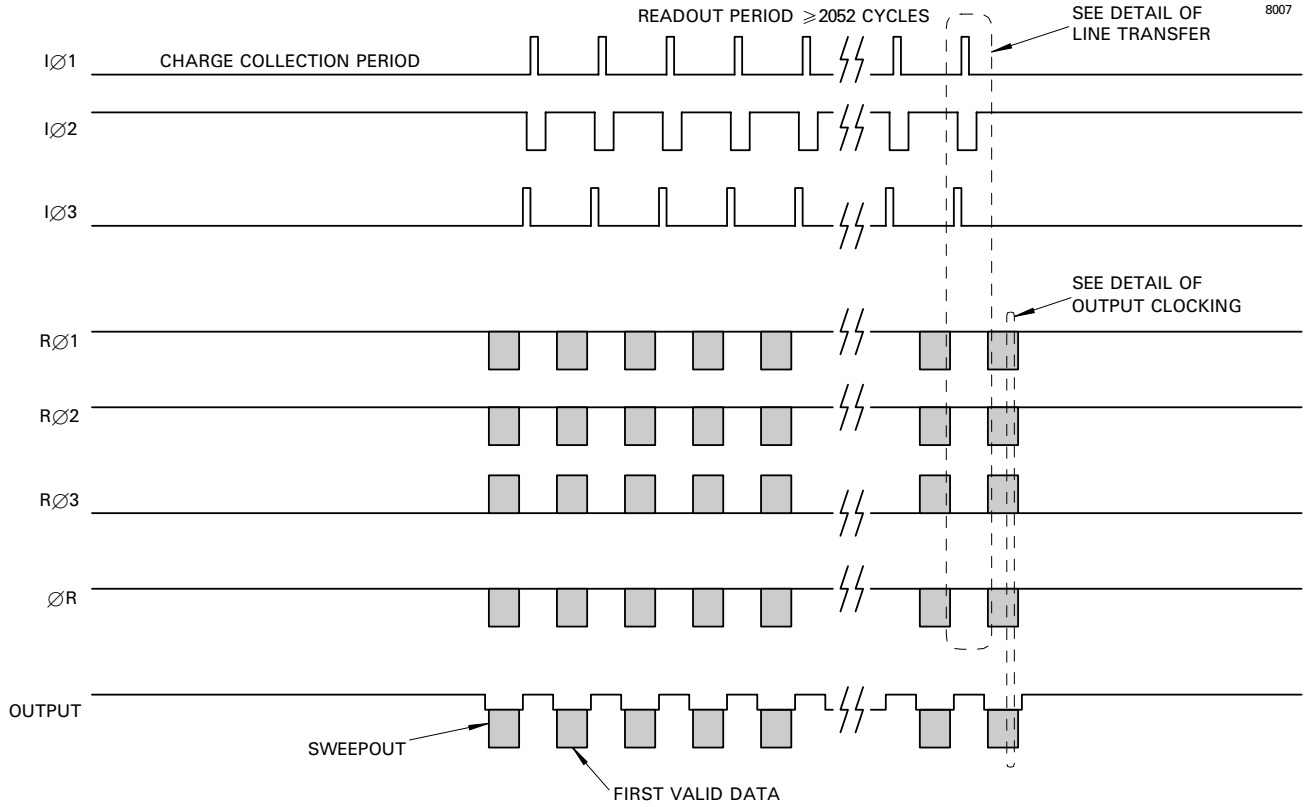
Maximum output transistor current 10 mA

NOTES

9. Not critical; OS = 3 to 5 V below OD typically. Connect to ground using a 3 to 5 mA current source or appropriate load resistor (typically 5 to 10 kΩ).
10. This gate is normally low. It should be pulsed high for charge dump.
11. OG2 = OG1 + 1 V for operation of the output in high responsivity, low noise mode. For operation at low responsivity, high signal, OG2 should be set high.
12. With the R∅ connections shown, the device will operate through both outputs simultaneously. In order to operate from the left output only, R∅1(R) and R∅2(R) should be reversed.

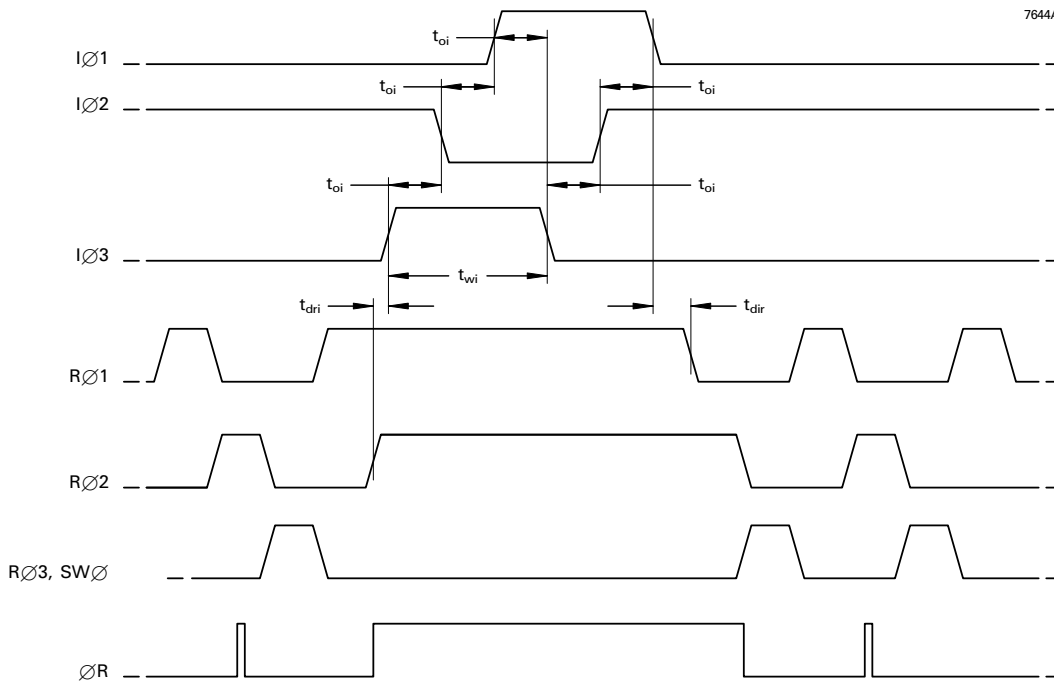
FRAME READOUT TIMING DIAGRAM

8007



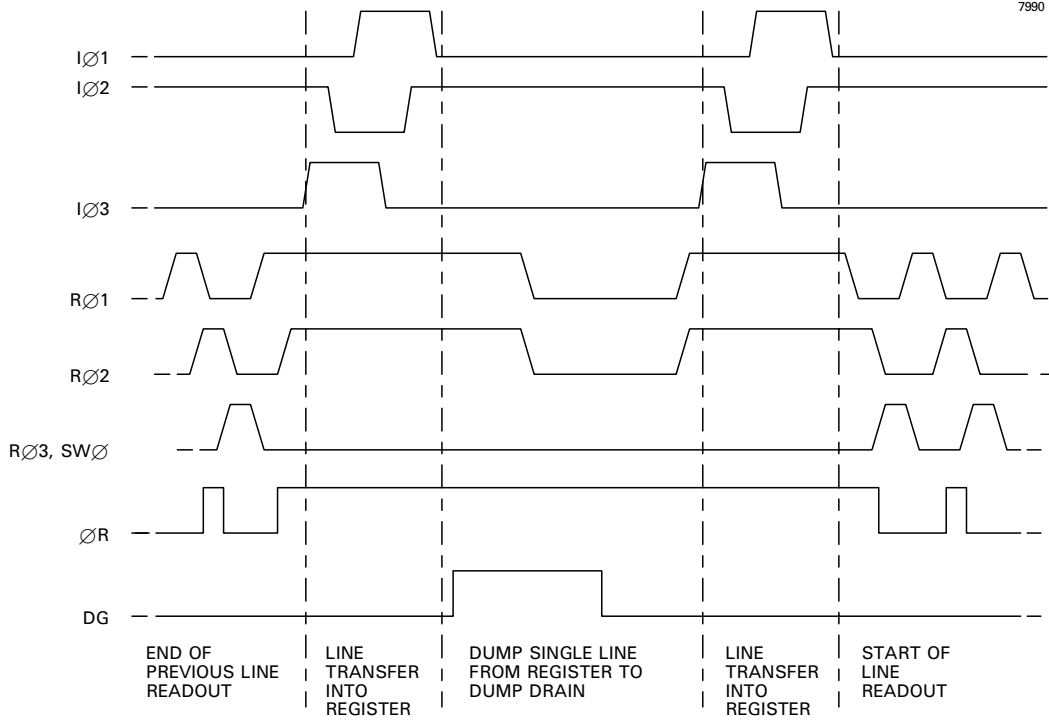
DETAIL OF LINE TRANSFER (Not to scale)

7644A



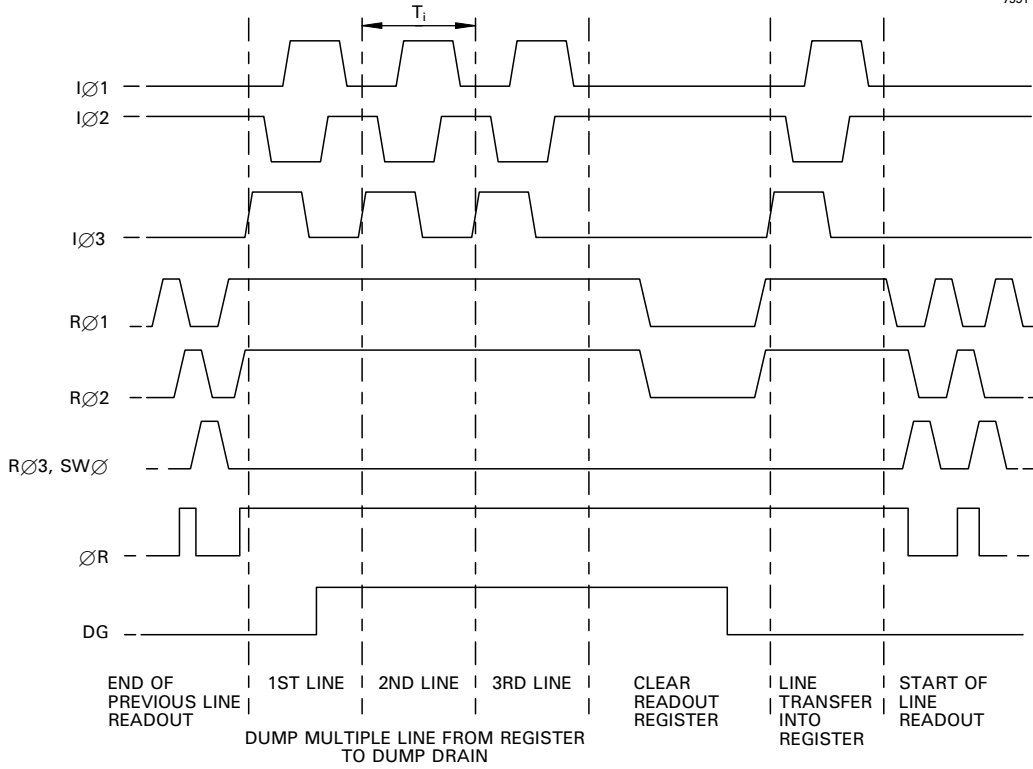
DETAIL OF VERTICAL LINE TRANSFER (Single line dump)

7990

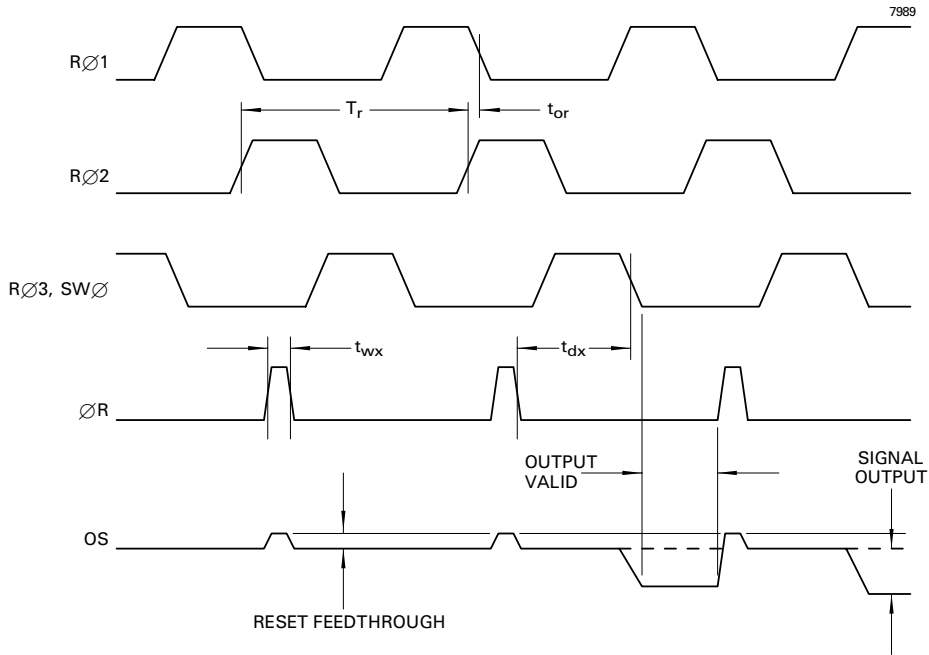


DETAIL OF VERTICAL LINE TRANSFER (Multiple line dump)

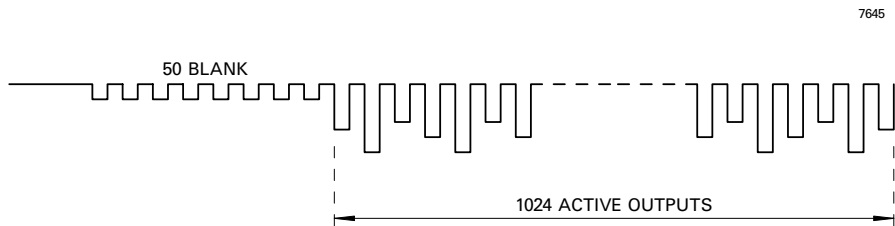
7991



DETAIL OF OUTPUT CLOCKING (Operation through both outputs)



LINE OUTPUT FORMAT (Split read-out operation)



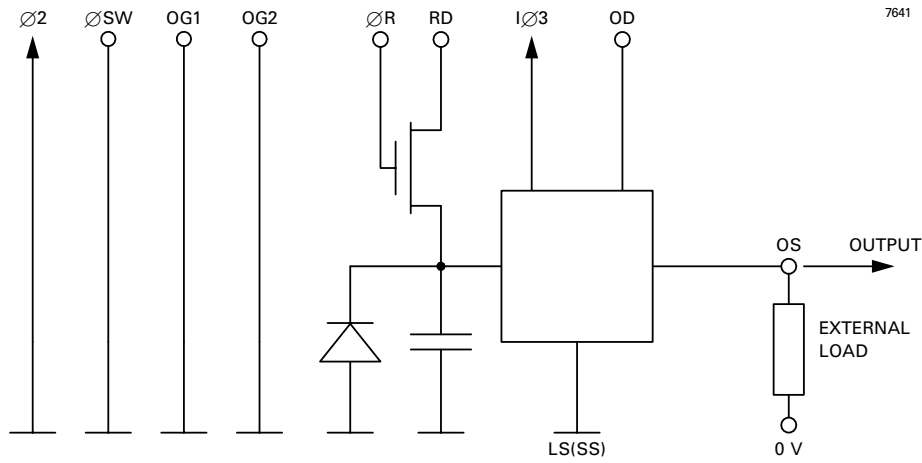
CLOCK TIMING REQUIREMENTS

| Symbol | Description | Min | Typical | Max | |
|------------------|---|-----------------------|-------------|-------------|---------------|
| T_i | Image clock period | 10 | 20 | see note 13 | μs |
| t_{wi} | Image clock pulse width | 5 | 10 | see note 13 | μs |
| t_{ri} | Image clock pulse rise time (10 to 90%) | 1 | 2 | $0.2T_i$ | μs |
| t_{fi} | Image clock pulse fall time (10 to 90%) | t_{ri} | t_{ri} | $0.2T_i$ | μs |
| t_{oi} | Image clock pulse overlap | $(t_{ri} + t_{fi})/2$ | 2 | $0.2T_i$ | μs |
| t_{dir} | Delay time, IØ stop to RØ start | 3 | 5 | see note 13 | μs |
| t_{dri} | Delay time, RØ stop to IØ start | 1 | 2 | see note 13 | μs |
| T_r | Output register clock cycle period | 300 | see note 14 | see note 13 | ns |
| t_{rr} | Clock pulse rise time (10 to 90%) | 50 | $0.1T_r$ | $0.3T_r$ | ns |
| t_{fr} | Clock pulse fall time (10 to 90%) | t_{rr} | $0.1T_r$ | $0.3T_r$ | ns |
| t_{or} | Clock pulse overlap | 20 | $0.5t_{rr}$ | $0.1T_r$ | ns |
| t_{wx} | Reset pulse width | 30 | $0.1T_r$ | $0.3T_r$ | ns |
| t_{rx}, t_{fx} | Reset pulse rise and fall times | 20 | $0.5t_{rr}$ | $0.1T_r$ | ns |
| t_{dx} | Delay time, ØR low to RØ3 low | 30 | $0.5T_r$ | $0.8T_r$ | ns |

NOTES

- No maximum other than that necessary to achieve an acceptable dark signal at the longer readout times.
- As set by the readout period.

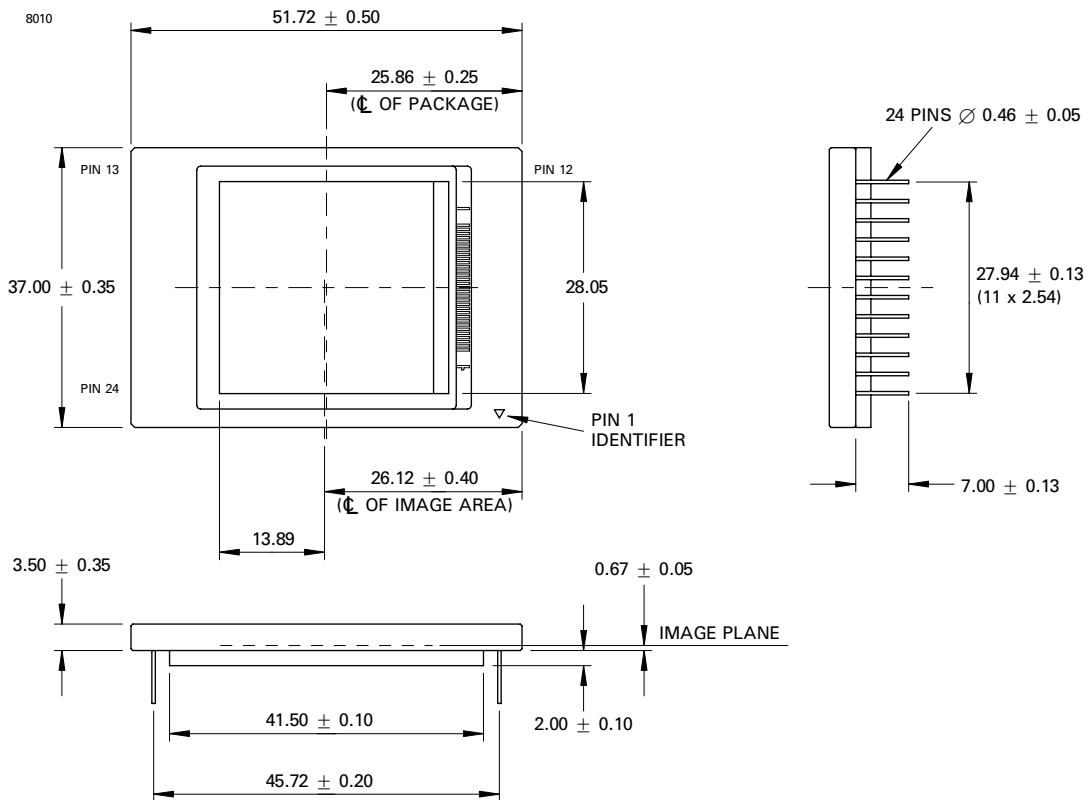
OUTPUT CIRCUIT



NOTES

- 15. The amplifier has a DC restoration circuit which is internally activated whenever IØ2 is high.
- 16. External load not critical; can be a 3 to 5 mA constant current supply or an appropriate load resistor.

OUTLINE (All dimensions in millimetres; dimensions without limits are nominal)



ORDERING INFORMATION

Options include:

- Temporary quartz window
- Temporary glass window
- Fibre-optic coupling
- UV coating
- X-ray phosphor coating

For further information on the performance of these and other options, please contact e2v technologies.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (pins 2, 7, 11, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23) but not to the other pins.

HIGH ENERGY RADIATION

Device parameters may begin to change if subject to an ionising dose of greater than 10^4 rads.

Certain characterisation data are held at e2v technologies. Users planning to use CCDs in a high radiation environment are advised to contact e2v technologies.

TEMPERATURE LIMITS

| | Min | Typical | Max | |
|---------------------|-----|---------|-----|---|
| Storage | 153 | - | 373 | K |
| Operating | 153 | 243 | 323 | K |

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling 5 K/min

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