CCD42-90 Scientific CCD Sensor Back-illuminated, 2048 x 4612 Pixels, Non Inverted Mode Operation

INTRODUCTION

The CCD42-90 is a large area full-frame (FF) imaging device. Back illumination technology, in combination with an extremely low noise amplifier, makes the devices well suited to the most demanding astronomical and scientific imaging applications.

DESCRIPTION

The device has an image area with 2048 x 4612 pixels each 13.5 µm square. There is a single read-out register with low-noise amplifiers at both ends. Additional JFET buffers are included in the package to provide an increased capability to drive high-capacitance loads. A gate-controlled dump-drain is provided to allow fast dumping of unwanted data. The register is designed to accommodate four image pixels of charge and a summing well is provided capable of holding that from six image pixels. The output amplifier has a feature to enable the responsivity to be reduced, allowing the reading of such large charge packets.

The device is supplied in a package designed to facilitate the construction of large close-butted mosaics used at cryogenic temperatures. The design of the package will ensure that the device flatness is maintained at the working temperature.

The sensor is shipped in a protective container, but no permanent window is fitted.

VARIANTS

Standard silicon and deep depletion silicon device types can be supplied with a range of AR coatings. Graded coatings are available as custom variants.

Mating ZIF sockets are available to order.

PART REFERENCES

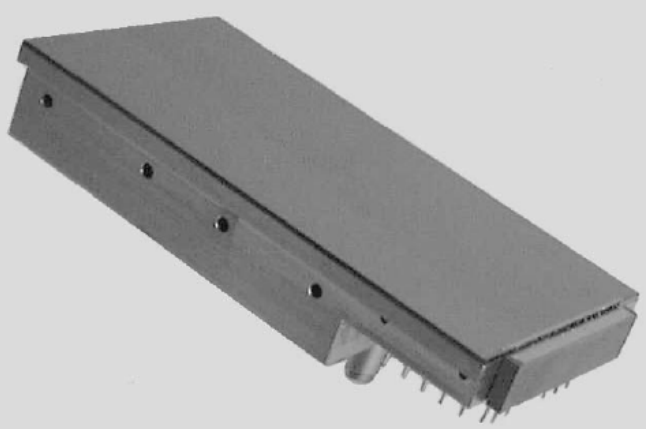
CCD42-90-g-xxx

g = cosmetic grade
xxx = device-specific part number

Details are given on the last page.

Devices with other formats (e.g. 2048 x 2048, 4096 x 4096 pixels) are also available in the same family.

Consult e2v technologies for further information on any of the above options.



SUMMARY PERFORMANCE
(Typical values)

Number of pixels	2048(H) x 4612(V)
Pixel size	13.5 µm square
Image area	27.6 mm x 62.2 mm
Outputs	2
Package size	28.2mm x 67.3 mm
Package format	Invar metal package with PGA connector
Focal plane height, above base	14.00 mm
Connectors	PGA; 40 pins
Flatness	15 µm p-v maximum
Amplifier responsivity	4.5 µV/e^-
Readout noise (rms)	3 e^- at 20 kHz
Maximum data rate	3 MHz
Image pixel charge storage	150,000 e^-
Dark signal at 173K	3 e^-/pixel/hour

Quoted performance parameters given here are “typical” values. Specification limits are shown later in this data sheet.

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A1A-100026, Version 9, December 2014
118717

PERFORMANCE at 173 K

Electro-Optical Specification (Note 1)

	Min	Typical	Max	Units	Note
Peak charge storage (image)	100k	150k	-	e^-/pixel	2a
Peak charge storage (register)	-	600k	-	e^-/pixel	2b
Output node capacity: OG2 low (mode 1) OG2 high (mode 2)	 - -	 300k 1,200k	 - -	 e^- e^-	2c
Output amplifier responsivity: OG2 low (mode 1) OG2 high (mode 2)	 3.0 -	 4.5 1.5	 -	 $\mu V/e^-$	3
Read-out noise (mode 1)	-	3	4	e^- rms	4
Maximum read-out frequency	-	1	3	MHz	5
Dark signal Specified at 173K [Equivalent 153K value]	 - -	 6	 182 [1]	 e^-/pixel/h	6
Charge transfer efficiency: parallel serial	 99.999 99.999	 99.9995 99.9998	 - -	 % %	7

NOTES

1. Device performance will be within the limits specified by “max” and “min” when operated at the recommended voltages supplied with the test data and when measured at a register clock frequency in the range 0.1 – 1.0 MHz. Most tests are performed at a nominal 500 kHz pixel rate. The noise as specified is separately measured in accordance with note 4.

2. (a) Signal level at which resolution begins to degrade.

   (b) Maximum register capacity.

   (c) Output node capacity under different modes.

3. For highest responsivity and lowest nose (mode 1), the voltage on OG2 should be 1V higher than that on OG1. For increased charge handling capacity, but with higher noise (mode 2), the voltage on OG1 should stay the same but the voltage on OG2 should be taken to about 20V.

4. Measured at OS with correlated double sampling at 20 kHz pixel rate in mode 1.

5. Depending on the external load capacitance to be driven. Higher loads (> 20 pF) can benefit from use of the optional JFET buffer. The register will transfer charge at higher frequencies, but performance cannot be guaranteed.

6. The dark signal is typically measured at a device temperature of 173K It is a strong function of temperature and the typical average (background) dark signal is taken as:

   $Q_d/Q_{do} = 122T^3e^{-6400/T}$

   where Q_{do} is the dark current at 293 K.

   Note that this is typical performance and some variation may be seen between devices. Dark current is lowest with the substrate voltage at +9 V, and somewhat higher with substrate at 0 V. However, Vss=0V is now recommended for highest spatial resolution; see note 9 later.

7. Measured with a ^{55}Fe X-ray source. The CTE value is quoted for the complete clock cycle (i.e. not per phase).

COSMETIC SPECIFICATIONS

Maximum allowed defect levels are indicated below.

	Standard silicon			Deep-depleted silicon		
Grade	**0**	**1**	**2**	**0**	**1**	**2**
Column defects (black or white)	2	6	12	2	6	12
White spots	300	450	800	500	1000	1500
Total spots (black and white)	900	1350	2000	1500	2000	2500
Traps > 200 e-	15	30	50	15	30	50

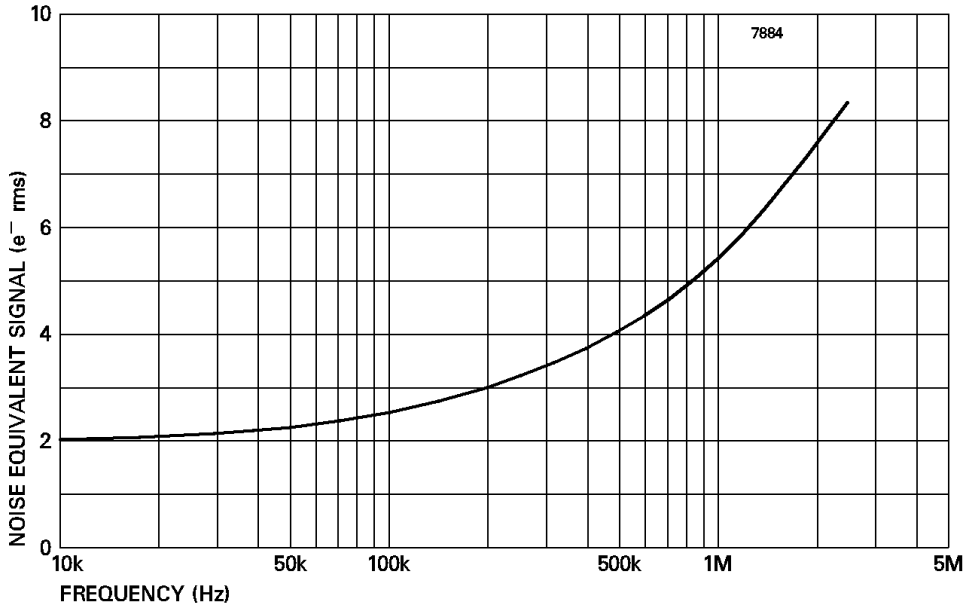
Grade 5 devices may also be available for set-up purposes. These are fully functional but with an image quality below that of grade 2, and may not meet all other specifications. Not all parameters may be tested.

DEFINITIONS

White spots	A defect is counted as a white spot if the dark generation rate is ≥ 5 e^-/pixel/s at 173 K. (which is also equivalent to ≥100 e^-/hour at 153 K). The temperature dependence is the same as for the mean dark signal; see note 6 above.
Black spots	A black spot defect is a pixel with a photo-response less than 50% of the local mean.
Column defects	A column is counted as a defect if it contains at least 100 white or dark single pixel defects.
Traps	A trap causes charge to be temporarily held in a pixel and these are counted as defects if the quantity of trapped charge is greater than 200 e^-
Defect exclusion zone	Defect measurements are excluded from the outer two rows and columns of the sensor.

TYPICAL OUTPUT AMPLIFIER NOISE

The variation of typical read noise with operating frequency is shown below. This is measured using correlated double sampling with a pre-sampling bandwidth equal to twice the pixel rate in mode 1, temperature range 150 – 230 K.

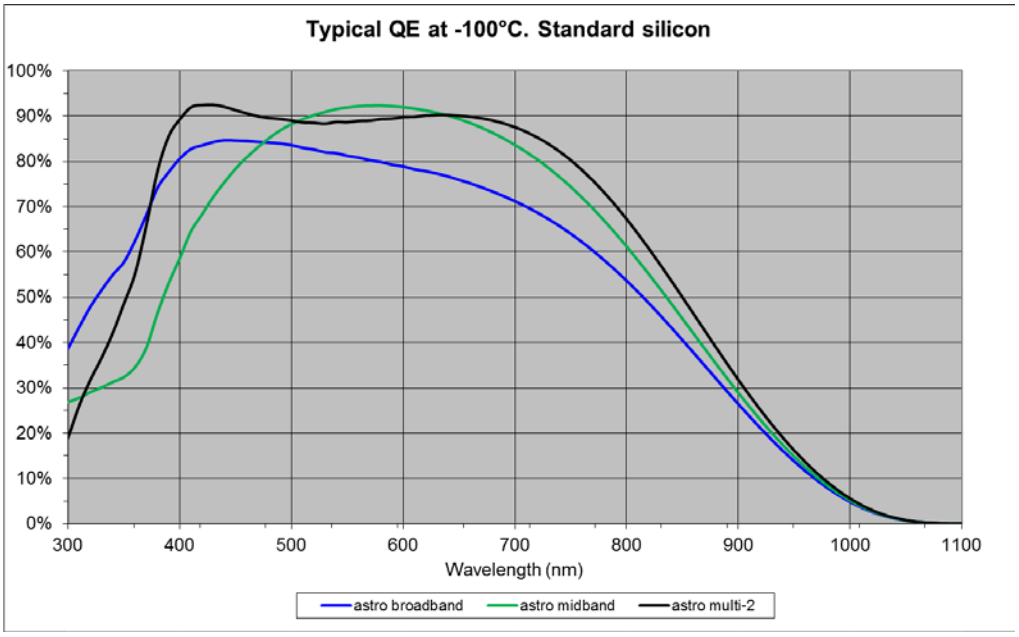


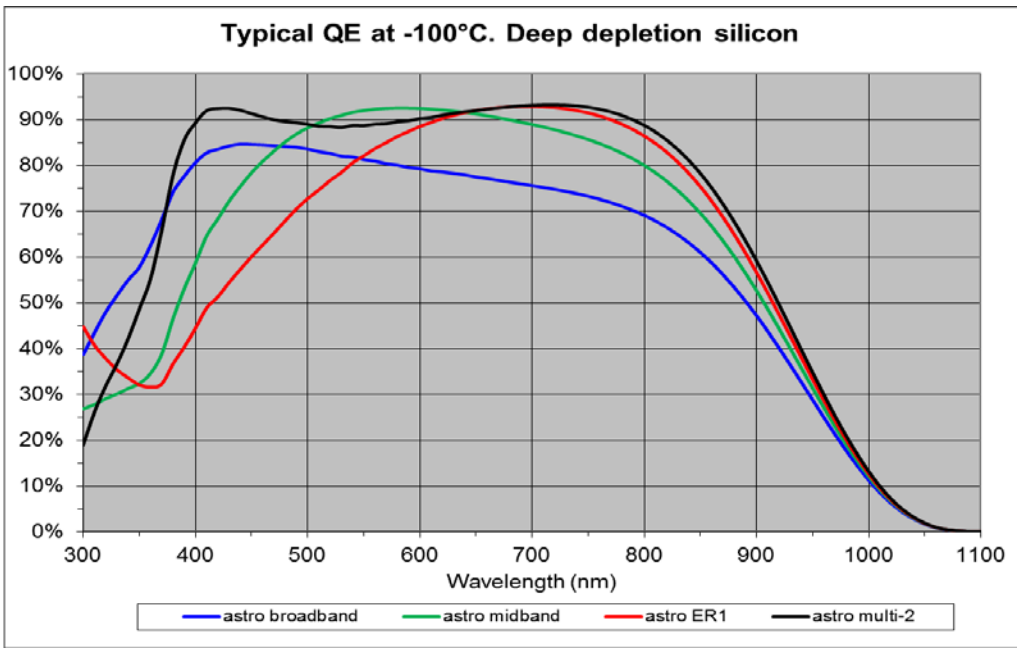
SPECTRAL RESPONSE

The table below gives guaranteed minimum values of the spectral response for several variants. PRNU is also shown.

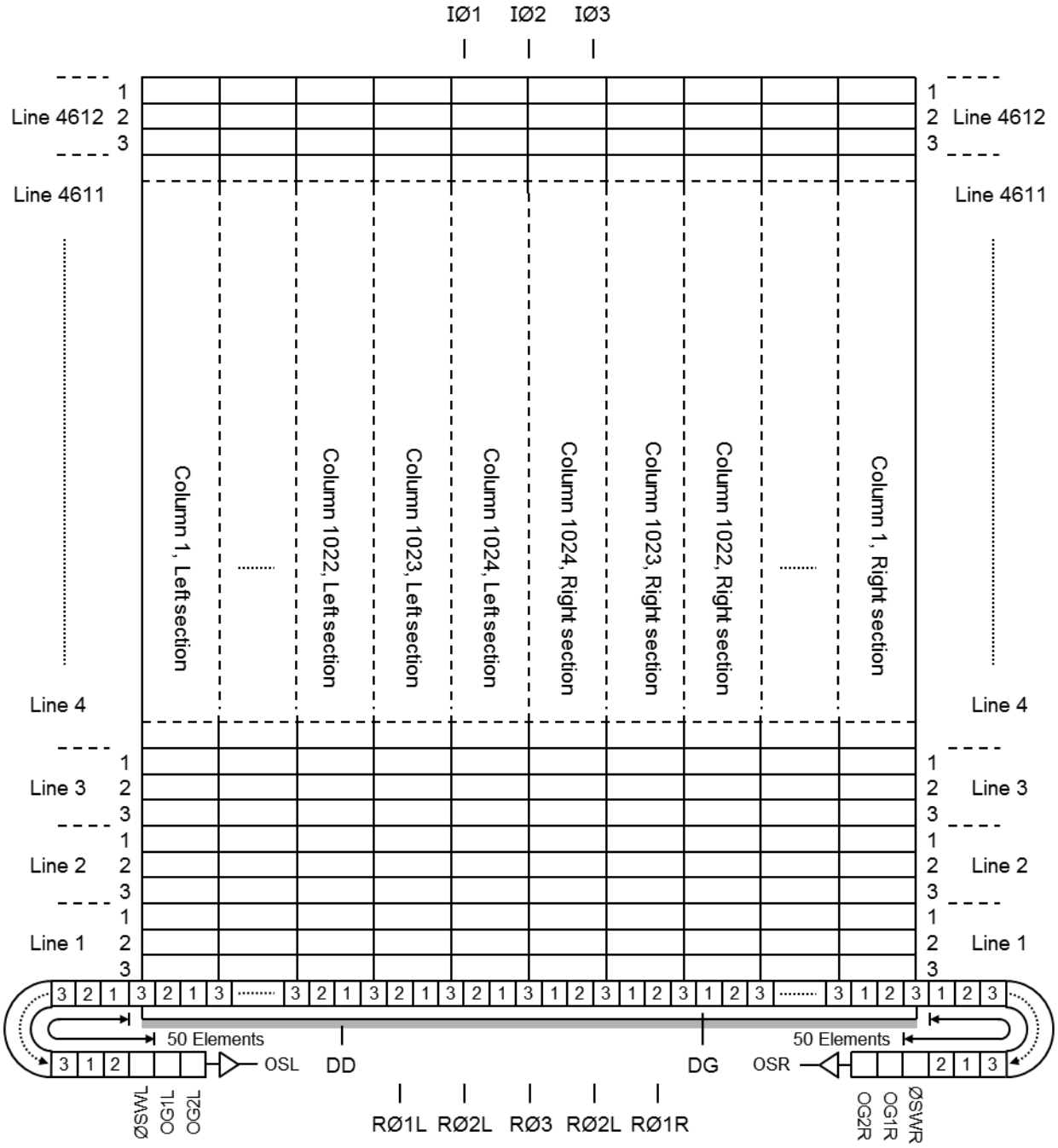
	Standard silicon Astro Broadband	Standard silicon Astro Midband	Standard silicon Astro Multi-2	Deep depletion silicon Astro Broadband	Deep depletion silicon Astro Midband	Deep depletion silicon Astro ER1 response	Deep depletion silicon Astro Multi-2	Maximum Pixel Response Non-Uniformity PRNU (1 σ) (%)
Wavelength (nm)	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	**Minimum QE (%)**	
350	40	20	30	40	20	20	30	-
400	70	50	75	70	50	35	75	3
500	80	80	75	75	80	65	75	-
650	75	80	80	70	80	80	80	3
900	25	25	25	40	40	45	50	5

See also the figures below. Consult e2v technologies for availability of spectral response variants. Devices with alternate spectral responses may be available to special order.





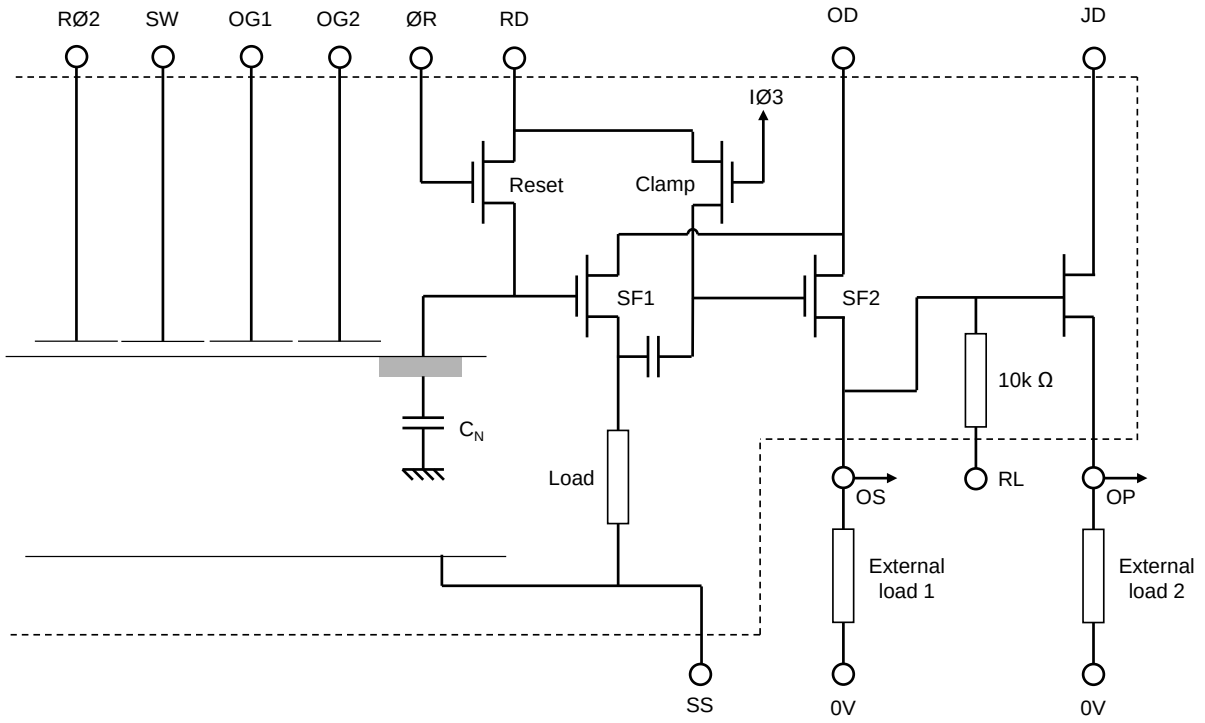
DEVICE ARCHITECTURE and ARRANGEMENT OF ELECTRODES



The device has a three-phase image area with a total of 2048(H) x 4612(V) pixels with connections IØ1, IØ2 and IØ3. The three-phase read-out register is of split configuration with connections RØ1L, RØ1R, RØ2L, RØ2R and RØ3. Adjacent to the register is a dump gate and drain structure with connections DG and DD, respectively. This may be used to dump unwanted lines of charges as they are transferred from the image section. At either end of the register are an additional 50 elements leading to the charge detection amplifiers. The last clocked electrodes are separately connected and designated ØSWL and ØSWR – these may be used for summing well purposes or simply clocked as RØ3.

The parallel to serial transfer is with the RØ1 and RØ2 phases held at clock 'high'. With the register connections as designated, a line of charges will be split between the two outputs. To transfer a whole line to the left-hand amplifier the connections to RØ1R and RØ2R should be transposed. To transfer a whole line to the right hand amplifier the connections to RØ1L and RØ2L should be transposed.

OUTPUT CIRCUIT



The device has a conventional output circuit with the output at OS. Within the package is an additional U309 JFET buffer amplifier for optional use, e.g. in cases where the external load capacitance is large (>> 20 pF). The connections for the left and right amplifiers are designated by the suffix (L) and (R), respectively, not shown above.

For most applications the output at OS will be used with external load 1 that can be either a 3 - 5 mA current source or a 5 - 10 kΩ resistor. RL, JD and OP and external load 2 are left unconnected. In this mode the output impedance is typically 300 Ω and the on-chip dissipation is typically 30 mW.

If only one amplifier is in use, then OD for the other amplifier can be left unconnected. RD should be connected with ØR clocked normally or held at clock high level.

If the JFET buffer is used then external load 1 is not connected, RL is connected to 0 V, JD is biased as specified, external load 2 can be either a 3 - 5 mA current source or a 5 - 10 kΩ resistor and the output is taken at OP. In this mode the output impedance is typically 100 Ω and the on-chip dissipation is typically 80 mW.

ELECTRICAL INTERFACE

CONNECTIONS, TYPICAL VOLTAGES AND ABSOLUTE MAXIMUM RATINGS

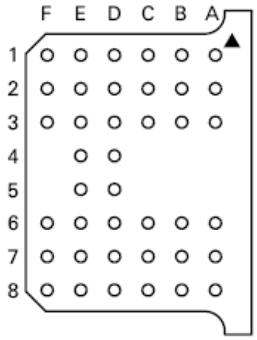
PGA PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see Note 8)			MAX RATINGS with respect to V_{SS} (V)
			Min	Typical	Max	
A1, A8, C1, C8, F2, F7	SS	Substrate	See Note 9			-
D8	IØ1	Image clock phase 1	8	10	15	±20
E8	IØ2	Image clock phase 2	8	10	15	±20
F8	IØ3	Image clock phase 3	8	10	15	±20
D4	RØ1 (L)	Register clock phase 1L	8	11	15	±20
E4	RØ2 (L)	Register clock phase 2L	8	11	15	±20
D5	RØ1 (R)	Register clock phase 1R	8	11	15	±20
E5	RØ2 (R)	Register clock phase 2R	8	11	15	±20
F6	RØ3	Register clock phase 3	8	11	15	±20
E3	ØR (L)	Reset gate L	9	12	15	±20
E6	ØR (R)	Reset gate R	9	12	15	±20
E2	ØSW (L)	Summing well gate L	9	11	15	±20
E7	ØSW (R)	Summing well gate R	9	11	15	±20
F3	DG	Dump gate (see Note 10)	-0.5	0	15	±20
D3	OG1 (L)	Output gate 1L	1	3	4	±20
D6	OG1 (R)	Output gate 1R	1	3	4	±20
B2	DD (L)	Dump drain	22	24	26	-0.3 to +30
B7	DD (R)	Dump drain	22	24	26	-0.3 to +30
D2	OG2 (L)	Output gate 2L	See Note 11			±20
D7	OG2 (R)	Output gate 2R	See Note 11			±20
B1	OD (L)	Output drain L	27	29	32	-0.3 to +35
B8	OD (R)	Output drain R	27	29	32	-0.3 to +35
A2	OS (L)	Output source L	See Note 12			-0.3 to +25
A7	OS (R)	Output source R	See Note 12			-0.3 to +25
C2	RD (L)	Reset drain L	15	17	19	-0.3 to +25
C7	RD (R)	Reset drain R	15	17	19	-0.3 to +25
Connections for optional U309 JFET (see note 13)						
A3	RL (L)	Load resistor L	Analogue ground (0V)			
A6	RL (R)	Load resistor R	Analogue ground(0V)			
B3	OP (L)	JFET source L				
B6	OP (R)	JFET source R				
C3	JD (L)	JFET drain L	OD (L)+2V			
C6	JD (R)	JFET drain R	OD (R)+2V			
Optional connections (Temperature sensor- see Note 14)						
D1, F1	Temp	Temperature sensor	Thermistor			
E1	NC	No Connection				

If all voltages are set to the typical values, operation should be obtained at or close to the specifications, but some adjustment within the minimum-maximum range specified may be required to optimise performance. Refer to the specific device test data provided with each device as this gives the optimised values obtained during testing.

NOTES

8. All pulse low levels should be within range 0 ± 0.5 V, except read-out register clocks about +1 V higher.
9. Devices can be operated with the substrate at either low (0V) or higher (9V) values. Low substrate is particularly recommended for deep-depletion variants, since it maximizes the depletion depth for best Point Spread Function. High substrate minimises the dark current.
10. Non-charge-dumping level is shown. For charge dumping DG should be pulsed to within 12 ± 2 V.
11. OG1 is typically set to 3 V. Then, for operation in the high responsivity, low noise mode 1, OG2 should be set 1 V higher at typically 4 V. For operation in the low responsivity, increased charge handling mode 2, OG2 should be set to +20 V.
12. Do not connect to voltage supply but use a 3 - 5 mA current source or a 5 - 10 kΩ external load connected to 0 V. The quiescent voltage on OS is then typically within a range 6 - 8 V above the RD voltage. The maximum current is 10 mA.
13. U309 data: VGD and VGS absolute maximum = -25V.
14. These connections are for an optional temperature sensor; consult factory for availability.

PIN CONNECTIONS (View facing underside of package)



ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances (defined at mid-clock level)

	Typical	Units
IØ/IØ inter-phase	10	nF
IØ/SS	25	nF
RØ/RØ	90	pF
RØ/SS	175	pF
ØR/SS	20	pF

Electrode series resistance

	Typical	Units
IØ	25	Ω
RØ	10	Ω

The total capacitance on each phase is the sum of the inter-phase capacitance to each of the adjacent phases and the capacitance of the phase to substrate.

POWER UP/POWER DOWN

When powering the device up or down, it is critical that any specified maximum rating is not exceeded. Specifically, the voltage for the amplifier drains (pins B1 and B8) must never be taken negative with respect to the substrate. Hence, if the substrate is to be operated at a positive voltage (e.g. to minimise dark current) then the drive electronics should have a switch-on sequence which powers up all the drains to their positive voltages before the substrate voltage starts to increase from zero.

It is also important to ensure that excess currents (see Note 12) do not flow in the OS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

Similarly, for powering down, the substrate must be taken to zero voltage before the drains.

POWER CONSUMPTION

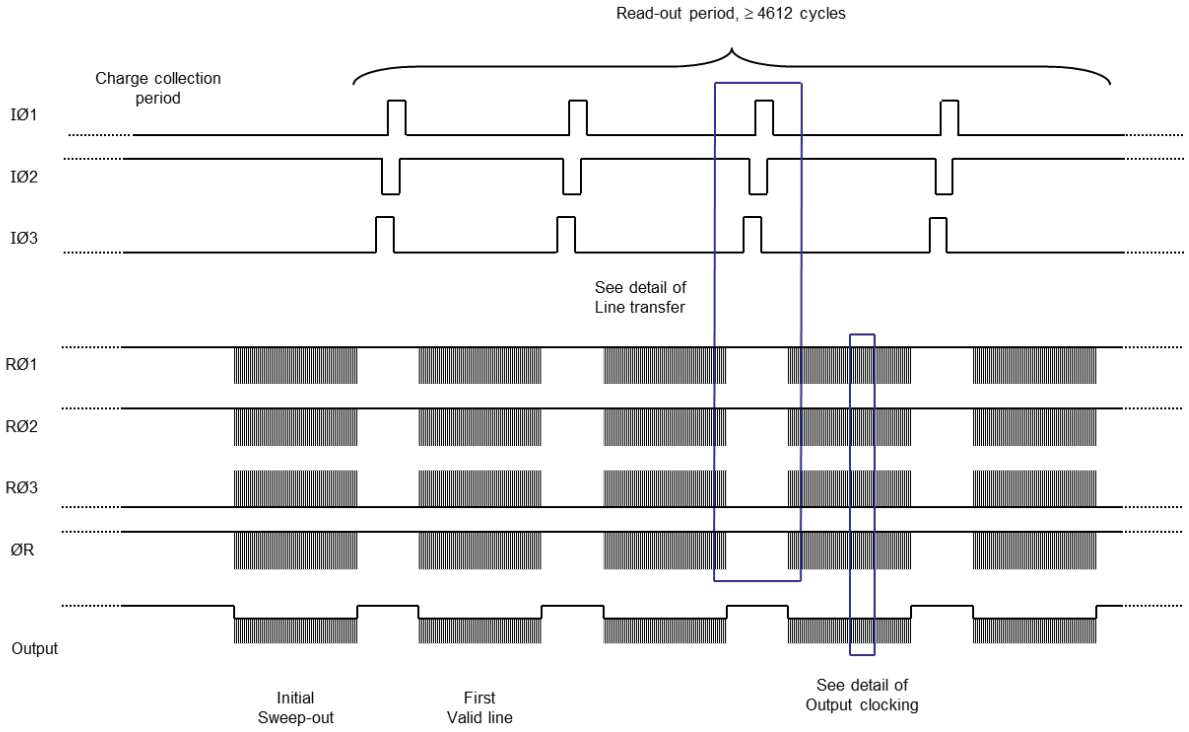
The power dissipated within the CCD is a combination of the static dissipation of the amplifiers and the dynamic dissipation from the parallel and serial clocking (i.e. driving the capacitive loads).

The table below gives representative values for the components of the on-chip power dissipation with continuous line-by-line read-out through one output (but with both amplifiers powered-up). The frequency is that for clocking the serial register.

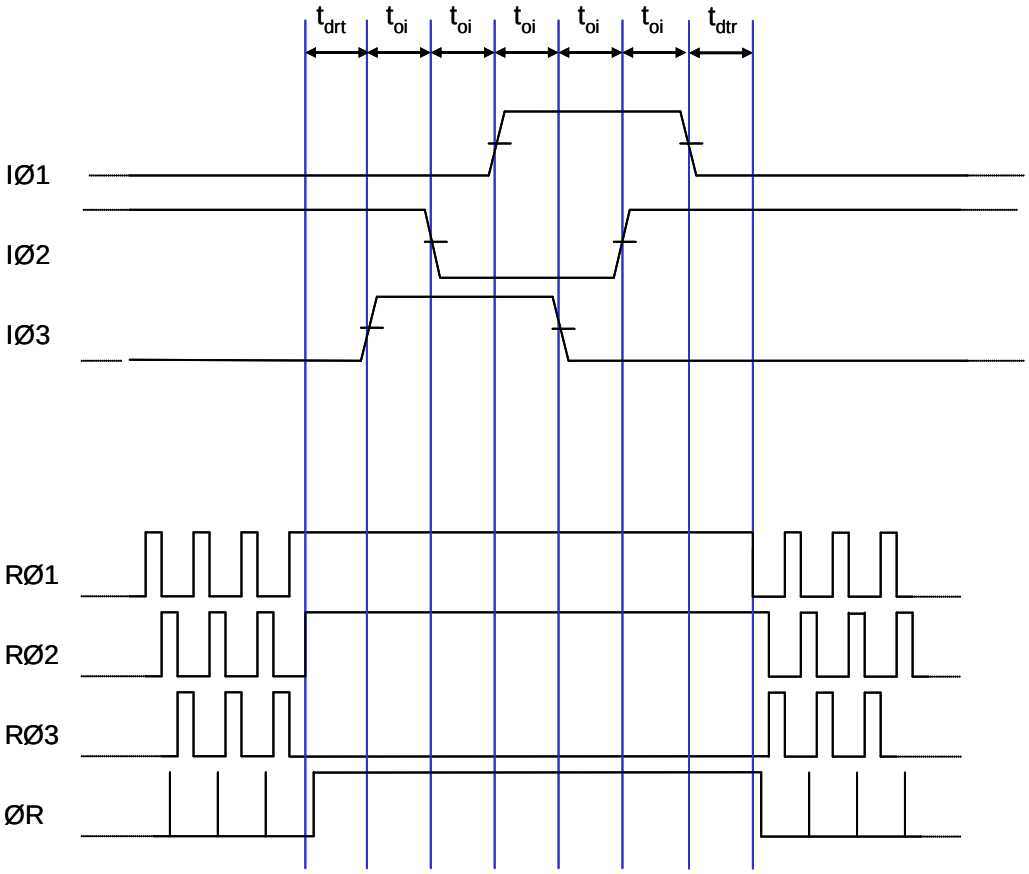
Read-out frequency	Line time	Power dissipation			
		Amplifiers	Serial clocks	Parallel clocks	Total
100 kHz	40 ms	60 mW	10 mW	1 mW	71 mW
1 MHz	4 ms	60 mW	100 mW	10 mW	170 mW

The dissipation reduces to only that of the amplifiers during the time that charge is being collected in the image sections with both the parallel and serial clocks static.

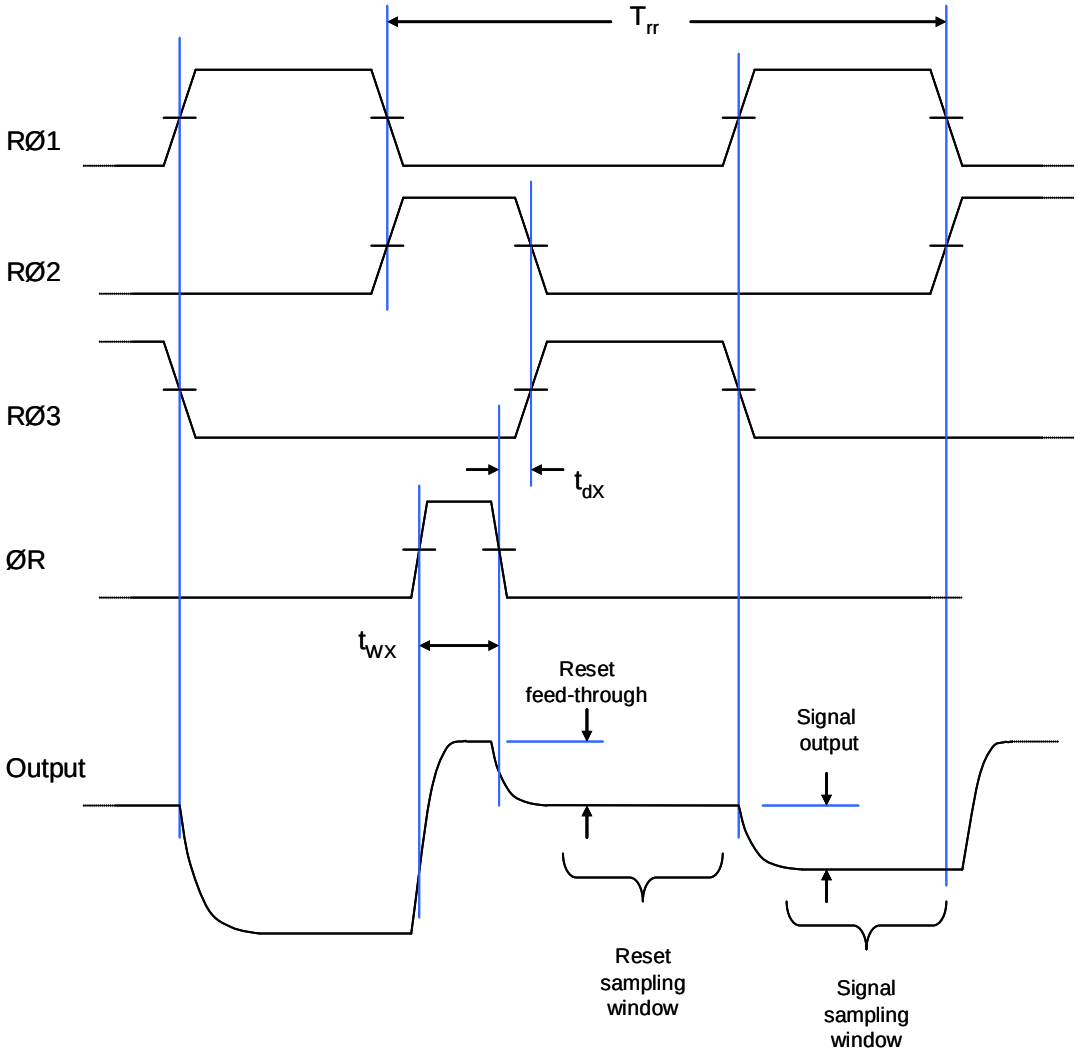
FRAME READOUT TIMING DIAGRAM



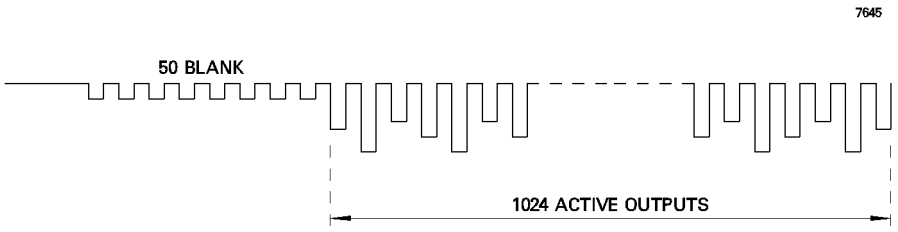
DETAIL OF LINE TRANSFER



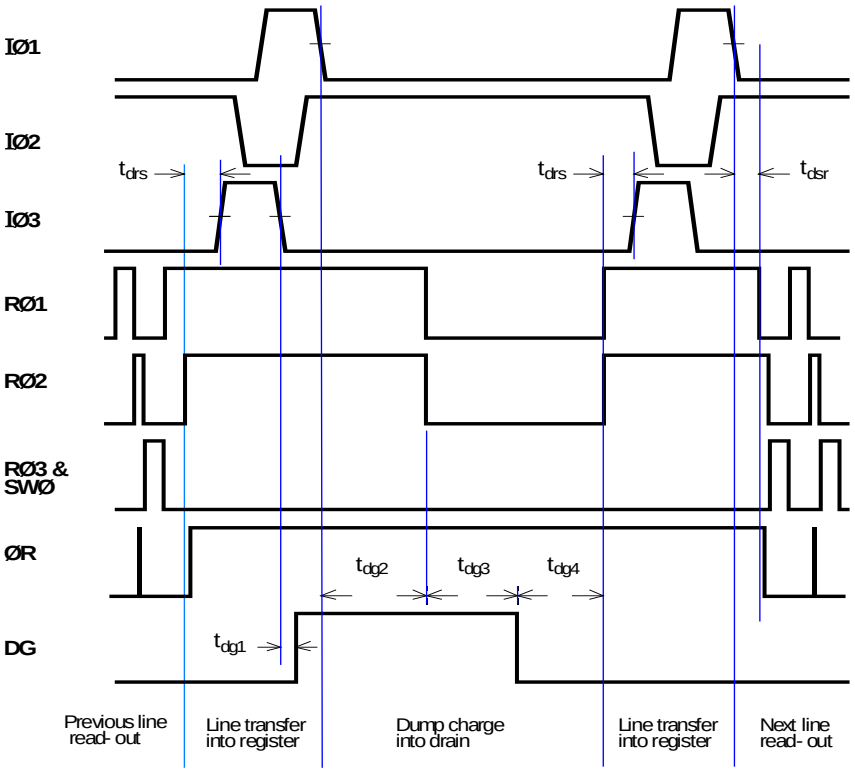
DETAIL OF OUTPUT CLOCKING



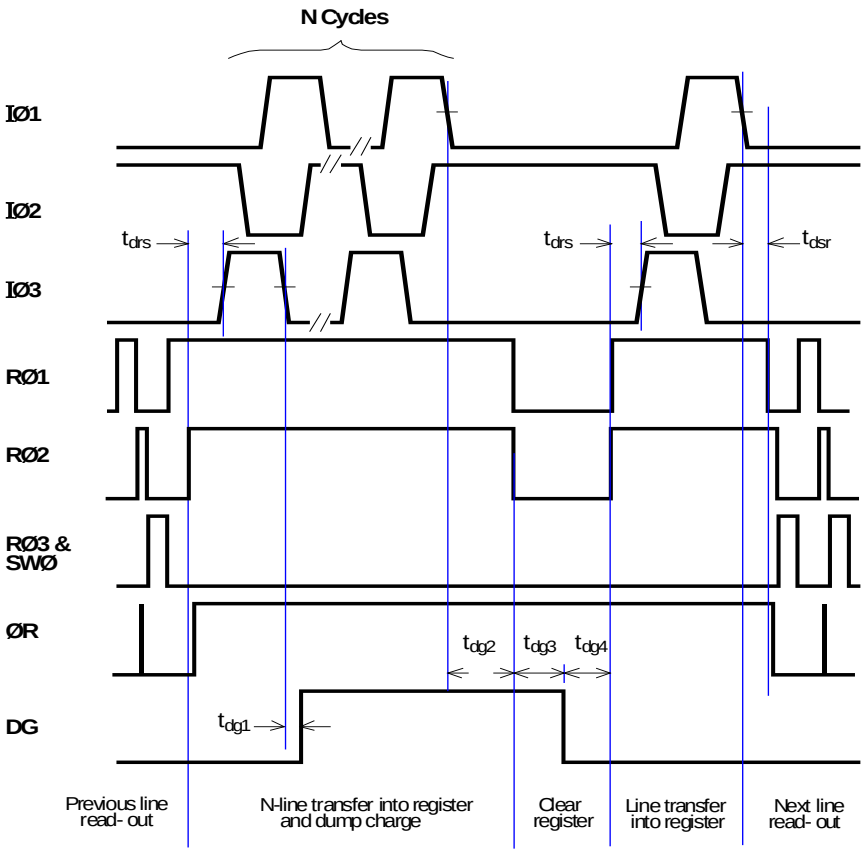
LINE OUTPUT FORMAT (Shown for split register operation)



DETAIL OF VERTICAL LINE TRANSFER (SINGLE LINE DUMP)



DETAIL OF VERTICAL LINE TRANSFER (MULTIPLE LINE DUMP)



CLOCK TIMING REQUIREMENTS

Symbol	Description	Minimum	Typical	Maximum	Units
t_{wi}	Image clock pulse width	$3t_{oi}$	50	(see Note 15)	µs
t_{ri}	Image clock pulse rise time (10 to 90%)	1	10	$0.5t_{oi}$	µs
t_{fi}	Image clock pulse fall time (10 to 90%)	t_{ri}	10	$0.5\ t_{oi}$	µs
t_{oi}	Image clock pulse overlap	5	10	$0.2T_i$	µs
t_{dir}	Delay time, IØ stop to RØ start	10	20	(see Note 15)	µs
t_{dri}	Delay time, RØ stop to IØ start	1	2	(see Note 15)	µs
T_{rr}	Output register clock cycle period	300	(see Note 16)	(see Note 15)	ns
t_{rr}	Register pulse rise time (10 to 90%)	50	$0.1T_r$	$0.3T_r$	ns
t_{fr}	Register pulse fall time (10 to 90%)	t_{rr}	$0.1T_r$	$0.3T_r$	ns
t_{or}	Register clock pulse overlap	50	$0.5t_{rr}$	$0.1T_r$	ns
t_{wx}	Reset pulse width	50	$0.1T_r$	$0.2T_r$	ns
t_{rx}	Reset pulse rise and fall times	20	$0.5t_{rr}$	$0.2T_r$	ns
t_{dx}	Delay time, ØR falling to RØ2 falling	0	20	40	ns
t_{dg1}	Delay time, IØ3 falling to DG rising	0	1	2	µs
t_{dg2}	Delay time, RØ1/2 falling to DG falling		$\geq t_{dir}$		µs
t_{dg3}	Delay time, IØ1 falling to RØ1/2 falling	2	5	10	µs
t_{dg4}	Delay time, DG falling to RØ1/2 rising	2	5	10	µs

NOTES

15. No maximum other than that necessary to achieve an acceptable dark signal at the longer read-out times.
16. As set by the read-out period.

PACKAGE DETAIL

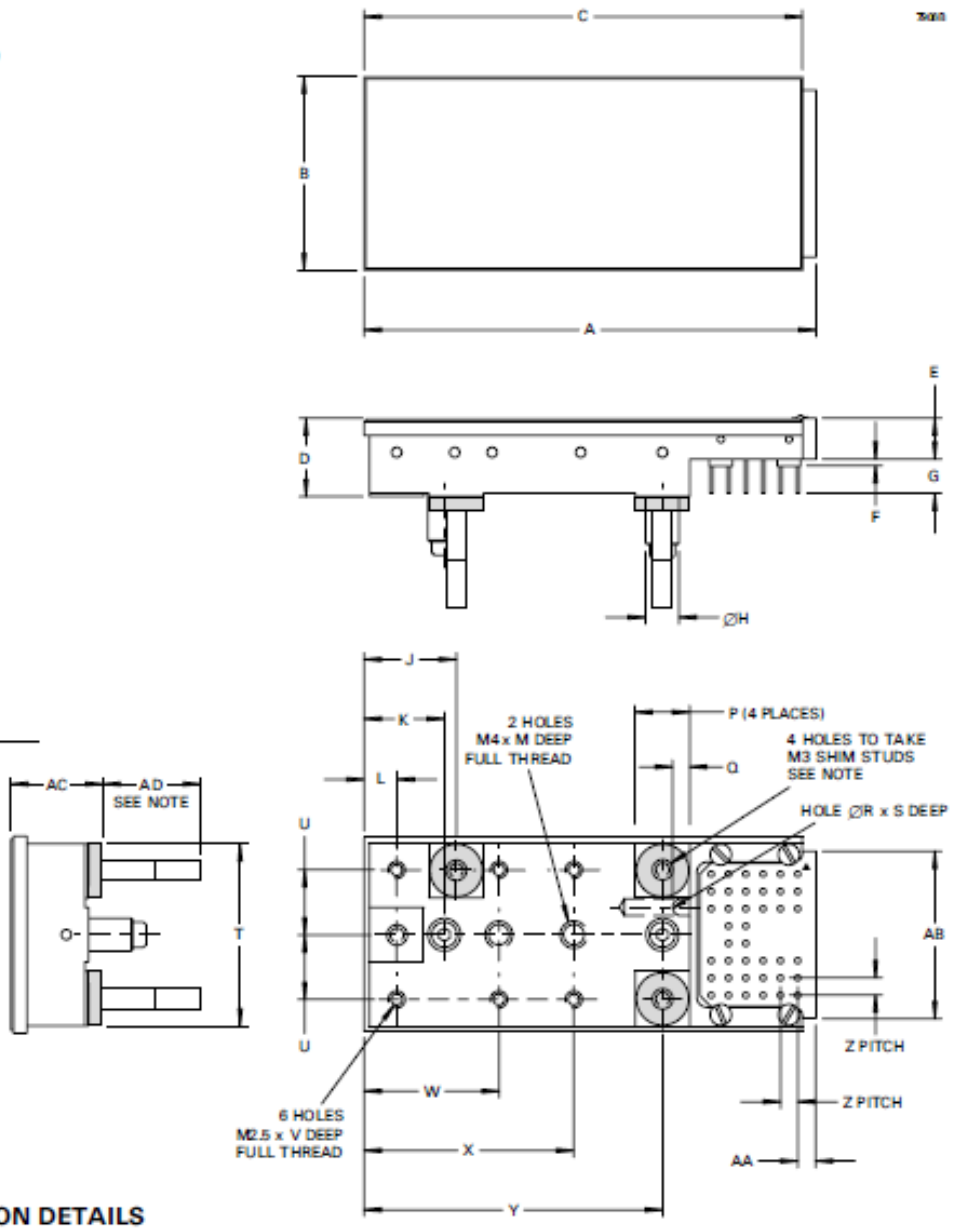
Package Mass = 150 g approx.

Inactive edge spacing

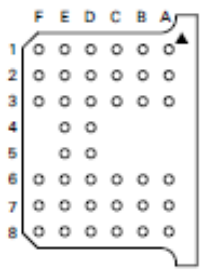
Sides	260 ± 50	µm
Top	120 ± 50	µm
Bottom (bond connections)	5.0	mm

OUTLINE
(All dimensions without limits are nominal)

Ref	Millimetres
A	67.32 max
B	28.168 ± 0.010
C	64.96 ± 0.01
D	11.65
E	6.00
F	1.00
G	5.00
H	4.800 ± 0.005
J	14.35
K	12.60
L	4.60
M	6.00 min
P	8.00
Q	2.50
R	2.50
S	6.50
T	27.00
U	9.50
V	5.50 min
W	20.60
X	31.60
Y	44.60
Z	2.54
AA	2.70
AB	24.50
AC	14.00 ± 0.01
AD	15.00 ± 0.01 8.50 ± 0.01



PIN CONNECTION DETAILS
(See page 5)



Outline Note

The device is supplied with shim studs to hold it onto the customer's mounting plate, fitted to three of the four holes as required. The studs are available in two lengths (see dimension AD). The default unless specified is the 15.00 mm stud in the offset position.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases, a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving sockets to be positively grounded

Evidence of incorrect handling will invalidate the warranty. All devices are provided with internal protection circuits to the gate electrodes (i.e. all CCD pins except SS, DD, RD, OD and OS) but not to the other pins.

The devices are assembled in a clean room environment. e2v technologies recommend that similar precautions are taken to avoid contaminating the active surface.

HIGH ENERGY RADIATION

Performance parameters will begin to change if the device is subject to ionising radiation. Characterisation data is held at e2v technologies with whom it is recommended that contact be made if devices are to be operated in any high radiation environment.

TEMPERATURE RANGE

Operating temperature range	153 - 323 K
Storage temperature range	73 - 373 K

Full performance is only guaranteed at the nominal operating temperature of 173 K.

Operation or storage in humid conditions may give rise to ice on the surface when the sensor taken to low ambient temperatures and this can easily cause irreversible damage.

Maximum rate of heating or cooling: 5 K/min.

PART REFERENCES

CCD42-90-g-xxx

g = cosmetic grade. Grade-1 is the default science grade. Grade-5 is a setup (engineering) grade.

xxx = device-specific part number; see below

Part Number	Description	
CCD42-90-g-B08	Standard silicon	Astro-midband
CCD42-90-g-B32	Deep depletion	Astro-Broadband
CCD42-90-g-B40	Standard silicon	Astro-Broadband
CCD42-90-g-F41	Deep-depletion silicon	Astro-midband
CCD42-90-g-G01	Deep depletion silicon	Astro multi-2

In all cases, consult e2v for availability.